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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/608,852	06/30/2000	Kiran A. Padwekar	042390.P5563	1971

7590 12/23/2003

Michael A DeSanctis
Blakely Sokoloff Taylor & Zafman LLP
12400 Wilshire Boulevard
7th Floor
Los Angeles, CA 90025

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/608,852	PADWEKAR, KIRAN A.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8,9 and 14-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8,9 and 14-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 8-9 and 14-20 and new claims 21-27 have been considered. Claims 1-7 and 10-13 have been cancelled as per Applicant's request. Claims 8, 14-15, and 18-20 have been amended as per Applicant's request. New claims 21-27 have been added.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "100" has been used to designate both a simplified instruction pipeline and a computer system. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: Please correct on page 14, line 22 from "Figure *6is* a flow diagram..." to read --Figure 6 is a flow diagram...--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8-9, 14-17, and 21-24 rejected under 35 U.S.C. 103(a) as being unpatentable over Stiles et al., U.S. Patent Number 5,515,518 (herein referred to as Stiles) in view of Karp et al., U.S. 6,321,328 (herein referred to as Karp).

6. Referring to claims 8 and 14, Stiles has taught a method comprising:

   a. Speculatively allocating a first branch entry for a conditional branch in a speculative branch target buffer (SBTB) prior to execution of the conditional branch responsive to decoding the conditional branch and finding no branch entry in an architectural branch target buffer (ABTB) corresponding to the conditional branch (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28);

   b. Speculatively allocating a second branch entry for the conditional branch in the SBTB (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28)

   c. Subsequently performing branch prediction for the conditional branch by determining a predicted target address branch based upon branch data associated with the second branch entry (Stiles Abstract; column 2, lines 21-61; and column 3; line 18 thru column 4, line 28).

7. Stiles has not explicitly taught:

   a. Speculatively allocating responsive to a subsequent failed attempt to locate a branch entry in the ABTB corresponding to the conditional branch (Karp Abstract and column 2, lines 1-55) and

   b. Allocating a third branch entry for the conditional branch in the ABTB after retirement of the conditional branch (Karp Abstract and column 2, lines 1-55).

8. However, Stiles has taught allocating branch entries (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28). Karp has taught:

a. Speculatively allocating responsive to a subsequent failed attempt to locate a branch entry in the ABTB corresponding to the conditional branch (Karp Abstract and column 2, lines 1-55) and

b. Allocating a third branch entry for the conditional branch in the ABTB after retirement of the conditional branch (Karp Abstract and column 2, lines 1-55).

9. Karp has taught, and a person of ordinary skill in the art would recognize, allocating data into a cache to decrease the stalls needed to access this information when it is not found in the current cache and updating the data after it has been executed and committed ensures the data being saved is correct and no longer has a chance of being incorrect (Karp column 2, lines 28-32). A person of ordinary skill in the art would have recognized that speculative allocating data and updating the data after it has been executed ensures there is no data corruption. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate speculatively allocating data and updating the data after it has been executed as taught by Karp in the device of Stiles to ensure no data corruption.

10. Referring to claims 9 and 15, Stiles has taught speculatively updating branch data associated with the first branch entry after said performing branch prediction for the conditional branch (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28).

11. Referring to claims 16 and 17, Stiles has taught a branch prediction circuit comprising:

a. A speculative branch target buffer (SBTB) cache having a plurality of branch entries to maintain speculative branch data associated with in-flight branches, the speculative branch data including a speculative history of taken/not-taken

outcomes (Applicant's claim 16) (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28) and

b. An architectural branch target buffer (ABTB) cache, coupled to the SBTB cache, the ABTB cache having a plurality of branch entries to maintain architectural branch data including the actual taken/not-taken outcomes (Applicant's claim 16) (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28).

12. Stiles has not explicitly taught:

a. ABTB associated to retired instructions (Applicant's claim 16); and

b. Wherein the first cache comprises a FIFO having entries corresponding to each of a plurality of pipeline stages of a microprocessor instruction pipeline (Applicant's claim 17).

13. However, Stiles has taught two caches (Stiles column 3, line 18 thru column 4, line 28), but not when they are exactly accessed and what type of cache they are. Karp has explicitly taught:

a. A first cache associated with in-flight instructions (Applicant's claim 16) (Karp Abstract and column 2, lines 1-55);

b. A second cache associated to retired instructions (Applicant's claim 16) (Karp Abstract and column 2, lines 1-55); and

c. Wherein the first cache means comprises a FIFO having entries corresponding to each of a plurality of pipeline stages of a microprocessor instruction pipeline (Applicant's claim 17) (Karp Abstract and column 2, lines 1-55).

14. Karp has taught, and a person of ordinary skill in the art would recognize, allocating speculative data into a first cache to decrease the stalls needed to access this information when it is not found in the second cache and entering the data into the second cache after the instruction has been executed and committed ensures the data being saved is correct and no longer has a chance of being incorrect (Karp column 2, lines 28-32). A person of ordinary skill in the art would have recognized that speculative allocating data and updating the data after it has been executed ensures there is no data corruption. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate speculatively allocating data and updating the data after it has been executed as taught by Karp in the device of Stiles to ensure no data corruption.

15. Referring to claims 21 and 22, Stiles has taught a processor comprising:

a. A fetch unit to speculatively retrieve instruction data for processing by an instruction pipeline (Applicant's claim 21) (Stiles column 4, lines 62-66 and Figure 2); and

b. A branch prediction circuit, coupled to the fetch unit, to predict final target addresses for branch instructions contained within the instruction data (Applicant's claim 21) (Stiles column 4, lines 62-66 and Figure 2), the branch prediction circuit including:

i. A speculative branch target buffer (SBTB) cache having a plurality of branch entries to maintain speculative branch data associated with in-flight branches, the speculative branch data including a speculative history of

taken/not-taken outcomes (Applicant's claim 21) (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28) and

ii. An architectural branch target buffer (A.BTB) cache, coupled to the SBTB cache, the ABTB having a plurality of branch entries to maintain architectural branch data including the actual taken/not-taken outcomes (Applicant's claim 21) (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28).

16. Stiles has not explicitly taught:

a. SBTB associated with in-flight branches (Applicant's claim 21);

b. ABTB associated to retired instructions (Applicant's claim 21); and

c. Wherein the first cache comprises a FIFO having entries corresponding to each of a plurality of pipeline stages of a microprocessor instruction pipeline (Applicant's claim 22).

17. However, Stiles has taught two caches (Stiles column 3, line 18 thru column 4, line 28), but not when they are exactly accessed and what type of cache they are. Karp has explicitly taught:

a. A first cache associated with in-flight instructions (Applicant's claim 21) (Karp Abstract and column 2, lines 1-55);

b. A second cache associated to retired instructions (Applicant's claim 21) (Karp Abstract and column 2, lines 1-55); and

c. Wherein the first cache means comprises a FIFO having entries corresponding to each of a plurality of pipeline stages of a microprocessor instruction pipeline (Applicant's claim 22) (Karp Abstract and column 2, lines 1-55).

18. Karp has taught and a person of ordinary skill in the art would recognize allocating speculative data into a first cache to decrease the stalls needed to access this information when it is not found in the second cache and entering the data into the second cache after the instruction has been executed and committed ensures the data being saved is correct and no longer has a chance of being incorrect (Karp column 2, lines 28-32). A person of ordinary skill in the art would recognize that speculative allocating data and updating the data after it has been executed ensures there is no data corruption. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate speculatively allocating data and updating the data after it has been executed as taught by Karp in the device of Stiles to ensure no data corruption.

19. Referring to claims 23 and 24, Stiles has taught:

a. Wherein the branch data includes a speculative history field representing the Speculative taken or not-taken history of the branch for a predetermined window of executions of the branch (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28), and

b. Wherein said speculatively updating branch data comprises updating the speculative history field to reflect the taken or not-taken status of its most recent execution (Stiles Abstract; column 2, lines 21-61; and column 3, line 18 thru column 4, line 28).

20. Claims 18-20 and 25-27 rejected under 35 U.S.C. 103(a) as being unpatentable over Stiles et al., U.S. Patent Number 5,515,518 (herein referred to as Stiles) in view of Karp et al., U.S. 6,321,328 (herein referred to as Karp) as applied to claims 1, 10, and 16 above, and further in view of Applicant's admitted prior art in the Background of the Invention (herein referred to as Prior Art).

21. Referring to claims 18-20 and 25-27, Stiles has not taught:

a. Wherein the SBTB cache comprises dual-ported (Applicant's claims 18 and 25);

b. Wherein the SBTB cache comprises single-ported (Applicant's claims 19 and 26); and

c. Wherein the ABTB cache comprises single-ported (Applicant's claims 20 and 27).

22. Prior Art has taught:

a. Wherein the SBTB cache comprises dual-ported (Applicant's claims 18 and 25) (Prior Art page 5, lines 1-5);

b. Wherein the SBTB cache comprises single-ported (Applicant's claims 19 and 26) (Prior Art page 5, lines 1-5); and

c. Wherein the ABTB cache comprises single-ported (Applicant's claims 20 and 27) (Prior Art page 5, lines 1-5).

23. As stated in Prior Art and known to a person of ordinary skill in the art, the reading/writing ports allow the SBTB to be accessed by the various pipeline stages for information (Prior Art page 5, lines 1-5) and it is necessary for the information to be available to the rest of the device for it to function properly. A person of ordinary skill in the art would have

recognized that the read/write ports allows the information to be accessed by the various pipeline stages and the rest of the device. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the read/write ports of Prior Art in the device of Stiles to allow information to be accessed by the various pipeline stages and the rest of the device.

Response to Arguments

24. Examiner withdraws the claim objections in favor of the amended and cancelled claims.

25. Examiner withdraws the drawing objections to Figures 1 and 3 in favor of the new drawings. However, Examiner could not locate replacement drawing 4A and the objection to the reference character "100" is maintained. Please see above for the full drawing objection.

26. Examiner withdraws the drawing objections to missing reference characters in the drawings and specification in favor of the new drawings and specification amendments.

27. Examiner withdraws the specification objection with regard to page 4, line 4 in favor of the specification amendment. However, Examiner maintains the objection with regard to page 12, line 22 since the error is still present. Please see above for the full specification objection.

28. Applicant's arguments filed 03 October 2003 have been fully considered but they are not persuasive.

29. Applicants argue on page 13 essentially

> "Stiles, for example, as acknowledged by the Examiner, does not teach or reasonably suggest an architectural branch target buffer (ABTB) or locating a branch entry in the ABTB corresponding to a conditional branch or allocating a

third branch entry in the ABTB for the conditional branch in the ABTB after retirement of the conditional branch..."

30. This has not been found persuasive. The Examiner did not acknowledge the reference does not teach an ABTB or "locating a branch entry in the ABTB corresponding to a conditional branch". The Examiner only acknowledged that Stiles did not teach "allocating a third branch entry in the ABTB for the conditional branch in the ABTB after retirement of the conditional branch". Stiles has taught an ABTB. The specification essentially states that an ABTB stores "architectural or actual branch data" (Specification page 7, lines 8-9). Stiles's caches and buffers store branch data, i.e. target addresses after the branch has been resolved and whether the branch has been taken or not (Stiles column 2, lines 21-61 and column 3, line 18 to column 4, line 28). Stiles has also taught "locating a branch entry in the ABTB corresponding to a conditional branch" in column 4, line 62 to column 5, line 5. As described by Stiles, the buffers are consulted for information about the current branch being processed.

31. Applicants argue on page 14 essentially

"Karp, like Stiles, does not teach or reasonably suggest an ABTB or allocating a third branch entry in the ABTB for the conditional branch in the ABTB after retirement of the conditional branch:..

Stiles, Karp, and Prior Art neither individually nor when combined, teach or reasonably suggest that ABTB or allocating a third branch entry in the ABTB for the conditional branch in the ABTB after retirement of the conditional branch"

32. This has not been found persuasive. Stiles has taught an ABTB and was not relied upon the teach "allocating a third branch entry in the ABTB for the conditional branch in the ABTB

after retirement of the conditional branch". Please see the rejection and response to arguments above. Karp was not relied upon to teach an ABTB and has taught "allocating a third branch entry in the ABTB for the conditional branch in the ABTB after retirement of the conditional branch". Karp has taught transferring data from a speculative buffer or cache to another buffer or cache when a instruction is committed, thereby eliminating contamination of bad data in the cache or buffer containing actual or architectural data (Stiles column 1, line 66 to column 2, line 55). A person of ordinary skill in the art would have recognized that committing an instruction is the same as retiring the instruction, because, in this case, committing the instruction occurs when the execution has completed. A system is certain that data contamination will not occur when the instruction is complete and ready to be committed or retired. Prior to the completion of an instruction, the data may be manipulated and changed, and, if the data were to be stored erroneously in the buffer or cache, it would contaminate the buffer or cache with bad data.

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Chung, U.S. Patent Number 5,774,710, has taught branch target buffers storing branch information.

34. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

35. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

37. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

38. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

December 22, 2003

RICHARD L. ELLIS
PRIMARY EXAMINER